PATENT
Docket No. 325772009100

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N. DeRiggi

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In the application of:

Kenji MASAKI

Serial No.: 09/287,530

Filing Date: April 7, 1999

For: DIGITAL IMAGE PROCESSING APPARATUS

Examiner: Barry Choobin

Group Art Unit: 2625

APPELLANT'S OPENING BRIEF

Commissioner for Patents
Washington, D.C. 20231

Sir:

This is a timely appeal from the final rejection of claims 1-15 and 21-24.

I. REAL PARTY IN INTEREST

The real party in interest is Minolta Co., Ltd.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences within the meaning of 37 CFR 1.192(c)(2) known to appellant or appellant's undersigned counsel.

III. STATUS OF CLAIMS

Claims 1-15 and 21-24 (reproduced in the attached Appendix) are pending in this application.

Claims 1-15 and 21-24 are finally rejected under 35 USC 102(b) as being anticipated by Yoshida (U.S. Patent No. 5,583,941).

IV. STATUS OF AMENDMENTS

No amendments have been submitted subsequent to the final rejection.

V. SUMMARY OF THE INVENTION

The invention is directed to digital image processing. It is desirable to track the changes made to images and save this information. However, it is important that the information which relates to the changes made to the image not make a visible influence on the image (specification page 4, lines 10-17). Thereby, bits for describing this type of information are placed in specific bit positions of pixel data at predetermined positions of the processed image data (page 4, lines 18-23). Since the specific bit positions are dispersed over the image surface, information about the changes made to the image during its processing can be embedded in the image without substantially influencing the quality of the image (page 4, line 23 through page 5, line 3). In this way, the history of the image processing is saved in the image itself (page 5, lines 4-6). This also has an added benefit in that the processing performed on the image can be reversed because the history of the processing has been saved (page 5, lines 14-17).

The contents of the image processing are assigned code numbers that can be represented in one byte, as shown in Fig. 3 (page 11, lines 8-10). For example, if the image processing is a contrast correction according to method 2, a code of 22 in hexadecimal notation is assigned (page 11, lines 10-13). The sequential arrangement of information can be seen in Fig. 4 and is explained at page 11, line 18 through page 12, line 16. To illustrate the operation of this invention as it is claimed, a full-color image which is 1280 x 1024 pixels is considered. If the image is divided by eight (8) in the horizontal and vertical directions into 64 (8 x 8) units, the central pixel in both the horizontal and vertical directions of each unit is used to embed information and bit positions are decided as shown in Fig. 5 (page 12, lines 2-13). In each position, the 44-bit information is embedded in the least significant bit positions of intensity data

of each pixel (page 12, lines 14-16). Since the processing information is dispersed in the manner described above and embedded in the least significant bit of the image data changes, there is no substantial reduction in image quality (page 13, lines 9-12).

VI. ISSUES PRESENTED FOR REVIEW

Whether the Examiner erred in rejecting claims 1-15 and 21-24 under 35 USC 102(b) as being anticipated by Yoshida.

VII. GROUPING OF CLAIMS

Claims 1-15 and 21-24 stand or fall together.

VIII. ARGUMENT

A. The rejection of claims 1-15 and 21-24 as anticipated by Yoshida should be reversed.

Claims 1-15 and 21-24 have been rejected under 35 USC 102(b) as anticipated by Yoshida.

Claim 1 recites "a processor, wherein the processor places bits for describing information different from information of image data obtained by image processing on original image data only in specific bit positions of multiple bits of pixel data only at predetermined positions of said processed image, each of the pixel data being expressed by using multiple bits." Since each pixel is an expression of multiple bits, bits of information can be placed within specific bit positions of pixel data without having to completely alter a pixel. For example, Appellant discloses calculating the least significant bit (LSB) positions of intensity data of each pixel and placing the image processing information within these bit positions (page 12, lines 14-16). In this way, the quality of the image is kept substantially unchanged, because the other bit positions of the pixel, the heavier weighted bits of the pixel, are left unchanged. Claim 1 recites that the processed image data is placed "only in specific bit positions of multiple bits of pixel data."

Appellant claims placing and obtaining "bits for describing information different from information of said first processed image data only in specific bit positions of multiple bits of pixel data only at predetermined positions of said processed image, each of the pixel data being expressed by using multiple bits." Accordingly, Appellant claims predetermining positions within a processed image and then placing information within only specific bit positions within only these predetermined positions.

For example, on page 12 of the specification, Appellant discloses dividing an image into 64 units and then using the central pixel of these units to embed information. The central pixel of these units would be an example of multiple bits of pixel data at predetermined positions of said processed image. Within these central pixels, information is placed in specific bit positions. For example, on page 12 of the specification, these specific bit positions are the least significant bit positions of intensity data of each of these central pixels.

Yoshida discloses an image processor which can prevent illegal copies of secret documents (col. 1, lines 65-67). Yoshida teaches a scramble means and a scramble cancel means (col. 2, lines 10-11). The scramble means rearranges pixel data in the document image read by a read means (col. 2, lines 12-15). More specifically, the pixel data of a document image is deformed according to prescribed rules of operation to be converted to an image which cannot be read (col. 3, lines 61-67). A matrix of pixel data of a document image is divided into minor matrices and adjacent four minor matrices are transposed according to these prescribed rules (col. 4, lines 8-12). The whole purpose of Yoshida is to modify the image so that it makes no sense when it is scrambled. The image is descrambled according to the scrambling rules.

Appellant respectfully submits that Yoshida fails to teach placing information only in specific bit positions of pixel data only at predetermined positions of said processed image, as claimed. The Examiner states that Fig. 6 in Yoshida shows the placement of bits in specific bit

positions ("Fig. 6 LSB corresponds to specific bit position.") (see Office Action dated February 26, 2002). However the Examiner is mistaken; Fig. 6 does not show placing information bits in a specific bit position. Fig. 6 is described in Yoshida at column 7, lines 17-32. As described in Yoshida, "Fig. 6 illustrates a situation when a block data is embedded in an image, one level (say "0") of a binarized data is expressed at a density which is the same as those of adjacent pixels, while the other level ("1" is expressed at a density which is different a little from those of adjacent pixels." Yoshida, column 7, lines 17-21. In Yoshida, information is not placed in any specific bit position, but rather, information is placed in a variety of different bit positions, which are influenced by adjacent pixels.

In response to this argument, the Examiner asserted that "specific bit position corresponds to Fig. 25, step 1312 of Yoshida" (see Advisory Action dated June 12, 2002). However, step 1312 of Yoshida discusses a process for confirming whether characteristic points have the predetermined positions in relation to the whole image. Applicants claim predetermining positions within the image and then placing information at specific bit positions **only within the predetermined positions**, not within the whole image.

In response to Appellant's argument, the Examiner asserted that Yoshida discloses that if the digital data cannot be embedded in such a way because of its long length, it is divided into blocks of a predetermined length, and the blocks are embedded (see Office Action dated January 15, 2003, item 1, page 2). The Examiner then asserts that a block number is added for each block in order to identify a position of a block in the digital image, and when the blocks are read, the blocks are rearranged in order of block number (referring to col. 7, lines 1-7 of Yoshida).

The Examiner seems to be asserting that since Yoshida discloses dividing blocks of data into "predetermined" length, this is the same as placing bits of data "only at predetermined positions of said processed image," as claimed in claim 1. Appellant does not follow the Examiner's reasoning in this regard. The word "predetermined" is being used in Yoshida to describe how the data is divided and not where it is placed. According to Yoshida, after the

blocks are divided into predetermined length, they are embedded. However, Yoshida does not disclose that the blocks are embedded only at predetermined positions of the processed image. Yoshida does provide for a way to identify the embedded blocks ("a block number is added for each block ...") but this not mean that the data is embedded only at a predetermined position. In fact, Yoshida actually teaches away from embedding the data only at a predetermined position because if the data were embedded in predetermined positions, it would not be necessary to assign block numbers to identify the position of the block.

The Examiner further asserts that Yoshida discloses that block data of a digital data can be embedded in an image at a desired position irrespective of position and direction of density data, and each dot of a digital data is so small not to be recognized with naked eyes (referring to col. 7, lines 45-48 and Fig. 25 of Yoshida).

First, the disclosure at col. 7, lines 45-48 does not relate in any way to that which is shown in Fig. 25. Fig. 25 shows the flow of extracting numerical values from characteristic points (col. 14, lines 62-63). In other words, Fig. 25 shows the descrambling portion of the invention. In addition, the Examiner quotes the following portion of Yoshida "[B]lock data of a digital data can be embedded in an image at a desired position irrespective of position and direction of density data" but fails to clearly illustrate to which of the claimed features this corresponds. The Appellant assumes that since the Examiner underlined the term "position" in this quote, he is asserting that the data can be placed at predetermined positions. This is not reasonable in light of the entire claim. Claim 1 recites "placing bits . . . only at predetermined positions of said processed image." However, Yoshida goes on to state "because the embedding position of a digital data is not definite . . . " (col. 7, lines 48-49). This contradicts the Examiner's assertion that the data can be placed only at predetermined positions in Yoshida and teaches away from the claimed invention.

Finally, at page 4 of the Office Action dated January 15, 2003, the Examiner goes into a discussion of Fig. 25, which as stated above, relates to the descrambling process. Appellant is at

a loss as to how this discussion even relates to the claimed process of placing the bit for describing information into the processed image. The Examiner is attempting to equate opposite processes in his argument. Thus, the features of claim 1 are neither taught nor suggested by Yoshida.

Claims 6, 11 and 21 recite substantially the same features as discussed above in connection with claim 1 and are allowable for the same reasons.

Claims 2-5, 7-10, 12-15, and 22-24 are allowable at least due to their respective dependencies.

CONCLUSION

For the foregoing reasons, Appellant respectfully requests that the rejection of claims 1-15 and 21-24 under 35 USC 102(b) be reversed.

In the event that the transmittal letter is separated from this document and the Patent and Trademark Office determines that an extension and/or other relief is required, appellant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. 325772009100.

Respectfully submitted,

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APPENDIX OF APPEALED CLAIMS

1. An image processing apparatus, comprising:

a processor, wherein the processor places bits for describing information different from information of image data obtained by image processing on original image data only in specific bit positions of multiple bits of pixel data only at predetermined positions of said processed image, each of the pixel data being expressed by using multiple bits.

2. An image processing apparatus according to claim 1, wherein said pixels are dispersed at a plurality of predetermined positions on said image.

3. An image processing apparatus according to claim 1, wherein said information different from information of said processed image data is information describing the contents of image processing performed on said original image data to obtain said processed image data.

4. An image processing apparatus according to claim 1, wherein said information different from information of said processed image data is information describing time when said image processing is performed on original image data to obtain said processed image data.

5. An image processing apparatus according to claim 1, wherein said information different from information for describing said processed image data is information describing time when said bits are placed.

6. An image processing method comprising:

obtaining first processed image data by performing image processing on original image data; and

placing bits for describing information different from information of said first processed image data only in specific bit positions of multiple bits of pixel data only at predetermined positions of said processed image, each of the pixel data being expressed by using multiple bits.

7. An image processing method according to claim 6, wherein said pixels are dispersed at a plurality of predetermined positions on said image.

8. An image processing method according to claim 6, wherein said information different from information of said first processed image data is information describing the contents of image processing performed on said original image data to obtain said first processed image data.

9. An image processing method according to claim 6, wherein said information different from information of said first processed image data is information describing time when said first step is performed.

10. An image processing method according to claim 6, wherein said information different from information of said first processed image data is information describing time when said second step is performed.

11. A recording medium in which a program for a computer is stored, wherein said program is one that enables the computer to perform the following processing:

placing bits for describing information different from information of image data, which is obtained by image processing on original image data, only in specific bit positions of multiple bits of pixel data only at predetermined positions of said processed image, each of the pixel data being expressed by using multiple bits.

12. A recording medium according to claim 11, wherein said pixels are dispersed at a plurality of predetermined positions on said image.

13. A recording medium according to claim 11, wherein said information different from information of said processed image data is information describing the contents of image processing performed on said original image data to obtain said processed image data.

14. A recording medium according to claim 11, wherein said information different from information of said processed image data is information describing time when said image processing is performed on original image data to obtain said processed image data.

15. A recording medium according to claim 11, wherein said information different from information of said processed image data is information describing time when said bits are placed.

21. An image processing method comprising:

obtaining processed image data by performing image processing on original image data; and

placing bits for describing information different from information of the processed image data in specific bit positions of pixel data at predetermined pixels of said processed image, each of the predetermined pixels of said processed image being separated by at least one pixel from the rest of the predetermined pixels.

22. An image processing apparatus according to claim 1, wherein the positions of pixels in which the bits are placed is decided in accordance with a predetermined procedure irrespective of pixel data.

23. An image processing apparatus according to claim 1, wherein the positions of pixels in which the bits are placed is predetermined fixed positions irrespective of pixel data.

24. An image processing apparatus according to claim 1, wherein the positions of pixels in which the bits are placed is a predetermined position.